A transistor level IR-drop based method to characterize an accurate and compact model of an IP for SoC level IR-EM analysis

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MOTIVATION

- Hard IPs (embedded memories etc.) with increased design complexity and power demand are occupying a significant share of real estate in the present generation SoCs.
- Power-grid model of these hard-IPs contains the current sink locations and their relative current strengths, power-grid network and decap value of the IP which is required for SoC level IR-drop EM sign-off analyses.
- For any power model, accuracy and compactness are the two most important parameters.
  - **Accuracy** depends on the realistic location and relative strength of the current sinks, and this impacts the QoR (Quality of Results).
  - **Compactness** depends on the number of nodes. Fewer number of nodes yields reduced run times, and this impacts the design cycle.
- The conventional non-simulation based power-grid models lacks accuracy and/or compactness.
- Hence there is a need for smart power-grid models, which is accurate and compact.
- A smart model is required to ensure that genuine IR drop/EM issues aren't overlooked and/or that the SoC is not over-designed due to false violations.
- This model will also give IP designers and SoC integrators a higher level of confidence on their IR drop budgeting.

We need an **accurate and light weight** power-grid model of an IP

CONVENTIONAL VIEW

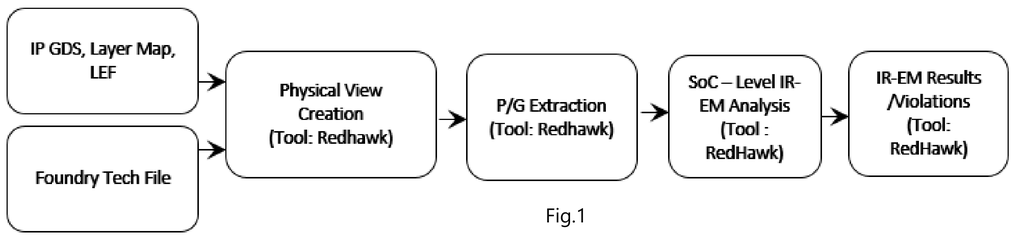


Fig.1

The conventional flow distributes current uniformly between the PG pins defined in the LEF/GDS or based on metal density of the target layer. This method will lead to unrealistic current distribution as the device-level diffusion layer currents are not simulated..

MAIN IDEA

DETAILED VIEW

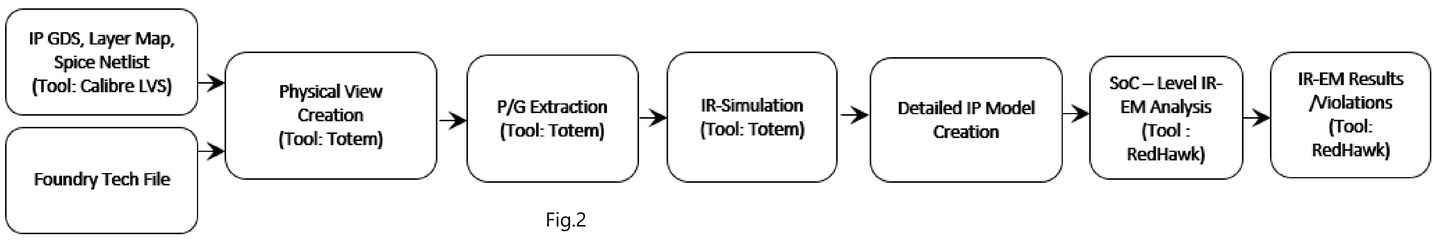


Fig.2

We propose an IR-drop simulation based method to characterize a power grid model for an accurate spatial current distribution and compactness as shown in Fig:2

Inputs are: "spice netlist with device locations" along with GDS, layer map and foundry technology files.

Current Assignment: **ACCURACY**

- The location of the current sinks on transistor pins are captured from a spice netlist which includes device coordinates.
- The relative strength of the current is derived based on the W/L ratio of the devices.

PG Extraction and Transistor level IR-drop Simulation

- After accurately assigning the current sinks on transistor diffusion layer pins, the voltage sources are defined on GDS/LEF top layer PG pins.
- Complete PG mesh is extracted to get the power grid connectivity.
- A transistor level static IR-drop analysis is done and current flow through each metal wires/vias is determined.

However, the above model is detailed as it creates current sinks on the BASE (OD) layers. The node count will cause higher tool runtimes. This model has to be optimized for node count.

SMART VIEW

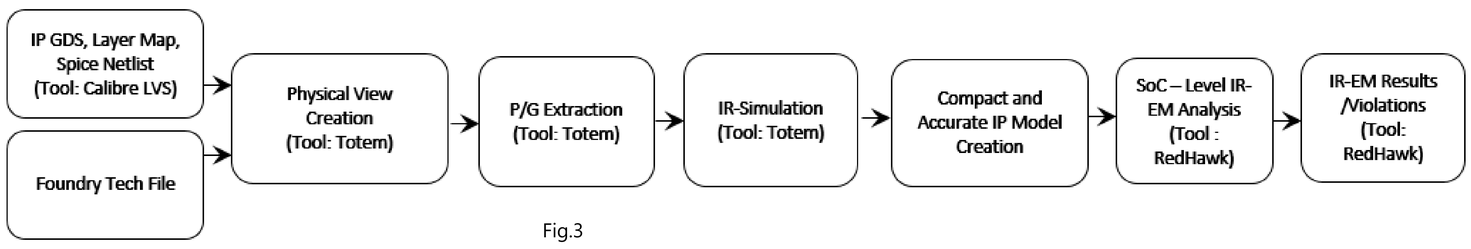


Fig.3

COMPACTNESS

- After IR-drop analysis is done, the current magnitude of each element on every layer down to diffusion is available. Now, the current sinks are re-assigned to the desired/target layer as specified in Fig:3.
- All the nodes/shapes of the layers below the target layer are removed. This pruning reduces the node count, without an impact on accuracy.

RESULTS

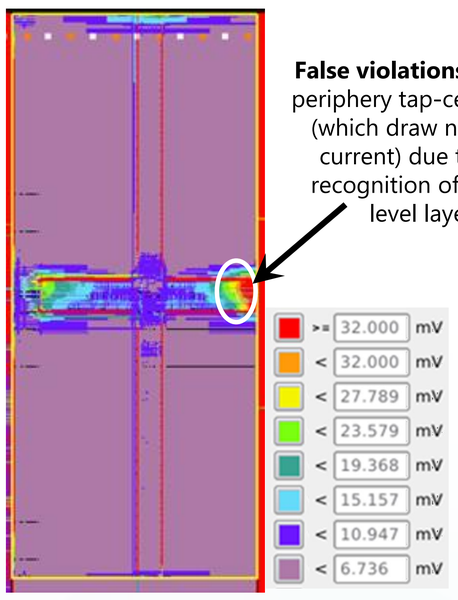
Memory	Detailed view (IR drop in mV)		Smart view (IR drop in mV)	
	Static	Dynamic	Static	Dynamic
MEM1_w02048x72b2c08	4.1	10.1	4.1	10.2
MEM2_w16384x072c16	2.1	5	1.9	5.1
MEM3_w02048x128b2c04	5.4	8	5.4	8.1
MEM4_w0512x072b1c02	5.6	10.7	5.7	11
MEM5_w08192x40b2c16	4.6	43.6	4.6	44.2
MEM6_w12288x72b8c08	4.6	9.1	4.4	9.9
MEM7_w32768x36b8c16	3.7	8.9	3.7	9.1

Table 1

	Compactness (Node Count)	Runtime	Accuracy
Conventional approach - Compact, but NOT accurate	5.96M	52 mins	Inaccurate (False violations)
Conventional approach - Accurate, but NOT compact	84.08M	4 hrs. 38 mins	Accurate (at huge runtime cost)
Smart approach - Compact and Accurate	19.24M	58 mins	**Accurate**

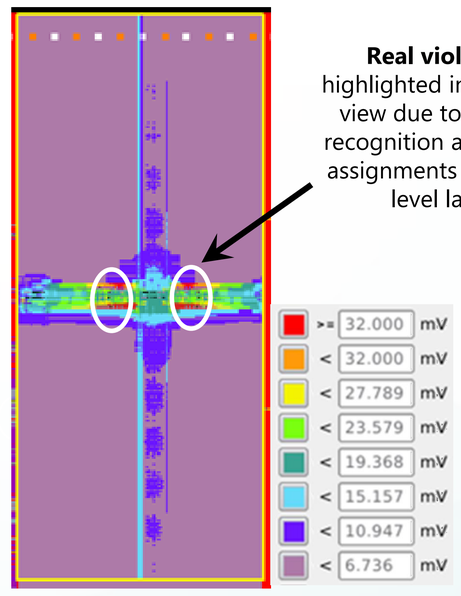
Table 2

Conventional View



False violations near the periphery tap-cell regions (which draw near zero current) due to non-recognition of device-level layers

Smart View



Real violations highlighted in the smart view due to accurate recognition and current assignments to device-level layers

Table 1 shows that the IR-drop results are comparable with the detailed accurate view.
Table 2 compares the node-count, runtime and accuracy, Smart view has superior runtime (due to reduced node count).

SUMMARY

A method is proposed for an accurate and light weight power-grid model for an IP which is required to sign-off SoC level power integrity analysis. This will avoid overdesign due to false violations and/or design failures as a result of overlooking potential issues. This model will also give IP designers and SoC integrators a higher level of confidence on their IR drop budgeting.